## REMARKS

Claims 1-15 and 17-30 have been examined on their merits.

Claim 16 remains withdrawn from consideration.

Claims 1-30 are all the claims presently pending in the application.

1. Claims 17-30 stand rejected under 35 U.S.C. § 101 as allegedly embracing or overlapping two different statutory classes of invention. Applicant respectfully traverses the rejection of claims 17-30 for at least the reasons set forth below.

Applicant herein editorially amends claim 17 to replace the phrase "and serving as" with more precise language. No new matter has been added by the amendments to claim 17. Applicant does not believe that the amendments to claim 17 narrow the literal scope of the claims. In addition, Applicant does not understand the Examiner's insistence that the phrase "serving as" somehow connotes a process limitation, especially when the phrase is used to clarify the operational relationships between several layers of semiconductor material. Moreover, the Examiner's reliance on MPEP § 2173.5(p) is not well taken. One of skill in the art would easily understand that the phrase "serving as" is indicative of the operational characteristics of the recited material layers, and that the phrase does not recite method steps of how to use the claimed device. Nevertheless, in order to expedite the prosecution of this application, Applicant has amended claim 17 to replace the phrase "serving as" with language similar to claim 1. Applicant notes that the Examiner did not reject claim 1 under 35 U.S.C. § 101.

Thus, Applicant believes that the Examiner's § 101 rejection has been overcome, and since there are no pending art-based rejections against claims 17-30, Applicant requests that the Examiner indicate claims 17-30 as allowable.

2. Claims 1-15 and 17-30 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. Applicant respectfully traverses the rejection of claims 1-15 and 17-30 for at least the reasons set forth below.

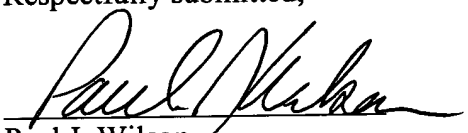
Applicant herein editorially amends claims 1, 3, 6, 14, 15, 17, 21, 29 and 30 to replace the phrase "first source of constant voltage" with the phrase "second terminal" in order to clarify that claims 1-15 and 17-30 are apparatus claims. Also, Applicant herein amends claims 1, 3, 6, 14, 15, 17, 21, 29 and 30 to differentiate between first and second terminals. No new matter has been added by the amendments to claims 1, 3, 6, 14, 15, 17, 21, 29 and 30. Applicant does not believe that the amendments to claims 1, 3, 6, 14, 15, 17, 21, 29 and 30 narrow the literal scope of the claims, since the claims remove the recitation of a constant voltage source. Applicant does not believe that independent claims 1 and 17 recite a method of using the claimed device. However, in order to expedite the prosecution of this application, Applicant herein amends claims 1, 3, 6, 14, 15, 17, 21, 29 and 30 to replace the phrase "first source of constant voltage" with the phrase "second terminal."

Thus, Applicant believes that the Examiner's § 112 rejection has been overcome, and since there are no pending art-based rejections against claims 1-15 and 17-30, Applicant requests that the Examiner indicate claims 1-15 and 17-30 as allowable.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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## APPENDIX

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE CLAIMS:**

**The claims are amended as follows:**

1. (*Thrice Amended*) A semiconductor device comprising:

a semiconductor substrate of one conductivity type;

shallow trench isolating regions having a first depth, and disposed in surface portions of said semiconductor substrate and defining active areas therebetween;

a first terminal connected to one of said active areas;

a second terminal [first source of constant voltage] connected to another of said active areas;

a circuit component connected between said first terminal and said second terminal [first source of constant voltage]; and

a protection circuit disposed adjacent to at least said one of said active areas, and comprising:

a first impurity region of said one conductivity type disposed adjacent to said at least one of said active areas, wherein said first impurity region is a base region of a bipolar transistor,

a second impurity region of a second conductivity type opposite to said one conductivity type disposed adjacent to said first impurity region, connected to said first terminal, wherein said second impurity region is one of an emitter region or a collector region of said bipolar transistor; and

a third impurity region of said other conductivity type connected to said second terminal [first source of constant voltage], wherein said third impurity region is the other of said emitter region or said collector region of said bipolar transistor.

3. (*Thrice Amended*) The semiconductor device as set forth in claim 2, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said second terminal [first source of constant voltage].

6. (*Thrice Amended*) The semiconductor device as set forth in claim 5, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said second terminal [first source of constant voltage].

14. (*Thrice Amended*) The semiconductor device as set forth in claim 1, wherein said first terminal is a signal output terminal, and said circuit component is an output transistor.

15. (*Thrice Amended*) The semiconductor device as set forth in claim 1, wherein said first terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said first terminal.

17. (*Twice Amended*) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a plurality of active areas disposed in a portion of said semiconductor substrate;

at least one shallow trench isolation region disposed between said active areas;

a first terminal connected to one of said active areas;

a second terminal [first source of constant voltage] connected to another of said active areas;

a circuit component connected between said first terminal and said second terminal [first source of constant voltage]; and

a protection circuit disposed adjacent to at least said one of said active areas, said protection circuit comprising:

a first impurity region of said first conductivity type disposed adjacent to at least one of said active areas, wherein said first impurity region is [and serving as] a base region of a bipolar transistor,

a second impurity region of a second conductivity type opposite to said first conductivity type disposed in said active area connected to said first terminal, wherein said second impurity region is [and serving as] one of an emitter region or a collector region of said bipolar transistor; and

a third impurity region of said second conductivity type connected to said second terminal [first source of constant voltage], disposed in another portion of said semiconductor substrate, wherein said third impurity region is [and serving as] the other of said emitter region or said collector region of said bipolar transistor.

21. (*Twice Amended*) The semiconductor device as set forth in claim 20, wherein said first impurity sub-region further comprises a second portion heavier in dopant concentration than said first portion and connected to said second terminal [first source of constant voltage].

29. (*Twice Amended*) The semiconductor device as set forth in claim 17, wherein said first terminal is a signal output terminal and said circuit component is an output transistor.

30. (*Twice Amended*) The semiconductor device as set forth in claim 17, wherein said first terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said first terminal.